This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for fabricating a non-volatile memory device, the method comprising:

providing a substrate;

forming an oxide layer overlying the substrate, the oxide layer having an amorphous surface structure;

forming a buffer layer ~~overlying~~ on the amorphous oxide layer after forming the oxide layer over the substrate;

thermally annealing the buffer layer to enhance an alignment of crystallites of the buffer layer;

forming a ferroelectric material overlying the substrate;

forming a gate layer overlying the ferroelectric material, the gate layer overlying a channel region; and

forming a first source/drain region adjacent to a first side of the channel region and a second source/drain region adjacent to a second side of the channel region.

2. The method of claim 1 wherein the channel region is about 1 micron and less.

3. The method of claim 1 wherein the ferroelectric material is a PZT bearing compound.

4. The method of claim 1 wherein the buffer layer is a magnesium bearing compound.

5. The method of claim 1 wherein the buffer layer is a magnesium oxide layer, the magnesium oxide layer being a barrier layer.

6. The method of claim 1 wherein the ferroelectric material has a thickness of less than about 1,000 Angstroms.

7. The method of claim 1 wherein the buffer layer has a thickness ranging from about 7 to 100 nanometers.

8. The method of claim 1 wherein the ferroelectric material has a thickness of about 100 Angstroms and greater.

9. The method of claim 1 wherein the ferroelectric material is PZT.

10. The method of claim 1 wherein the buffer layer is a barrier diffusion layer, the barrier diffusion layer substantially preventing diffusion between the ferroelectric material to the substrate.

11. The method of claim 1 wherein the buffer material is sputtered from a substantially pure magnesium target to form a magnesium oxide layer.

12. The method of claim 11 wherein the sputtering is maintained at a temperature greater than about 400 degrees Celsius or greater than about 500 degrees Celsius.

13. (Previously Amended) The method of claim 11 wherein the buffer layer is thermally annealed at a temperature of 800-1000 degrees Celsius for about 30 minutes.

14. The method of claim 1 wherein the ferroelectric material is highly oriented.

15. The method of claim 14 wherein the highly oriented material is a polycrystalline film.

16. (Previously Amended) The method of claim 1 wherein the ferroelectric material is substantially free from an amorphous structure.

17. The method of claim 15 wherein the polycrystalline film has a crystal structure of 100 angstroms and greater.

18. (Previously Amended) The method of claim 1 wherein the buffer layer is a template to provide an oriented growth of the ferroelectric material.

19. (Previously Amended) The method of claim 1 wherein the oxide layer is provided by a dry oxidation process comprising an oxygen bearing compound.

20. (Previously Amended) The method of claim 1 wherein the oxide layer passivates the surface of the substrate to protect the channel region.

21. (Currently Amended) A method for fabricating a non-volatile memory device, the method comprising:

providing a semiconductor substrate;

forming a gate oxide layer ~~first buffer layer overlying~~ on the substrate, the oxide layer having a non-crystalline structure;

forming a ~~second buffer~~MgO layer overlying the oxide layer after forming the oxide layer on the substrate ~~first buffer layer~~;

thermally annealing the second buffer layer to enhance an alignment of crystallites of the second buffer layer;

forming a ferroelectric material overlying the substrate;

forming a gate layer overlying the ferroelectric material, the gate layer overlying a channel region; and

forming first and second doped regions adjacent to first and second ends of the channel region.

22. Canceled.

23. The method of claim 21, wherein the oxide layer has an amorphous structure and the MgO layer has a crystal structure. ~~first buffer layer is an amorphous layer, and the second buffer layer is a highly-oriented layer.~~

24. The method of claim 23, wherein the second buffer layer has a thickness of no more than 10 nm.

26. The method of claim 21 wherein the second buffer layer is thermally annealed at a temperature of 800-1000 degrees Celsius.

27. (New) The method of claim 21, wherein the MgO layer formed on the oxide layer is provided with a highly-oriented structure.

28. (New) The method of claim 27, wherein the MgO layer has a polycrystalline structure prior to the annealing step.

29. (New) A method for fabricating a non-volatile memory device, the method comprising:

providing a semiconductor substrate;

forming an oxide layer on the substrate, the oxide layer having a non-crystalline structure;

forming a MgO layer on the oxide layer, the MgO layer formed on the oxide layer having a highly-oriented structure;

forming a ferroelectric material overlying the substrate;

forming a gate layer overlying the ferroelectric material, the gate layer overlying a channel region; and

forming first and second doped regions adjacent to first and second ends of the channel region.

30. (New) The method of claim 29, further comprising:

thermally annealing the highly-oriented MgO layer to enhance an alignment of crystallites of the of the MgO layer.

31. (New) The method of claim 29, wherein the MgO layer is formed after the oxide layer is formed on the substrate.

32. (New) A method for fabricating a non-volatile memory device, the method comprising:

providing a semiconductor substrate;

forming an amorphous gate dielectric layer on the substrate;

forming a MgO layer on the amorphous dielectric layer after forming the dielectric layer on the substrate, the MgO layer having a highly-oriented structure; and

forming a ferroelectric layer overlying the MgO layer,

wherein the dielectric layer, MgO layer and ferroelectric layer are patterned to form a transistor.

33. (New) The method of claim 32, wherein the MgO layer has a crystalline structure.

34. (New) The method of claim 33, wherein the MgO has a polycrystalline structure.

REMARKS/ARGUMENTS

Claims 1-21 and 23-34 are pending. Claims 1, 21 and 23 have been amended. Claim 22 has been canceled. New claims 27-34 have been added.

Claims 1, 3-10 and 14-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hirai and Kirin. Applicant respectfully traverses the rejection.

Claim 1 is directed to forming a non-volatile memory device. The claim recites "providing a substrate; forming an oxide layer overlying the substrate, the oxide layer having an amorphous surface structure; forming a buffer layer on the amorphous oxide layer after forming the oxide layer over the substrate; thermally annealing the buffer layer to enhance an alignment of crystallites of the buffer layer; forming a ferroelectric material overlying the substrate; forming a gate layer overlying the ferroelectric material, the gate layer overlying a channel region; and forming a first source/drain region adjacent to a first side of the channel region and a second source/drain region adjacent to a second side of the channel region."

The claimed embodiment relates to forming a buffer layer on the oxide layer that has been formed on the substrate. That is, a silicon oxide layer is formed on silicon surface using a thermal oxidation process without any prior deposited material on the silicon surface. An oriented, insulating buffer layer is formed on an amorphous silicon-oxide layer, rather than on silicon surface that has a crystalline structure. This process is based on the inventor's discovery that a certain insulating material (such as MgO) can be grown self-oriented on amorphous surface (such as silicon oxide) under certain process conditions, contrary to the general belief by those skilled in the art. The above process enables a silicon oxide layer to be formed directly on a silicon surface, so that high-quality passivation of silicon surface may be obtained.

However in Hirai et al., an oriented buffer layer is first formed on crystalline silicon surface and then a silicon oxide layer is formed sandwiched in between the silicon and insulating buffer by annealing them in oxygen ambient. A silicon oxide resulting from the Hirai process is generally of lower quality than the silicon oxide formed directly on the silicon surface. Hirai discloses the above method resulting in low quality oxide presumably because the inventors of Hirai, like others, did not know how to form an oriented buffer layer on a non-

crystalline surface. Kirin does not remedy the deficiency of Hirai. Therefore, claim 1 is allowable.

Claim 21 recites, "providing a semiconductor substrate; forming a gate oxide layer on the substrate, the oxide layer having a non-crystalline structure; forming a MgO layer overlying the oxide layer after forming the oxide layer on the substrate; thermally annealing the second buffer layer to enhance an alignment of crystallites of the second buffer layer; forming a ferroelectric material overlying the substrate; forming a gate layer overlying the ferroelectric material, the gate layer overlying a channel region; and forming first and second doped regions adjacent to first and second ends of the channel region." Neither Hirai nor Kirin, alone or in combination, disclose or teach the above recited features. Therefore, claim 21 is allowable.

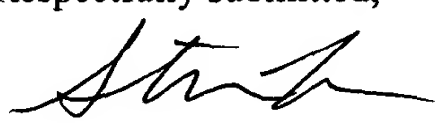
Claim 26 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hirai, Kirin, and Wolf. Applicants respectfully traverse the rejection. Claim 26 depends from claim 21 and is allowable at least for this reason.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



Steve Y. Cho
Reg. No. 44,612

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: 650-326-2400
Fax: 415-576-0300
SYC:syc
PA 3312461 v1